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10/655,964	09/04/2003	Mike Cogdill	200207753-1	8913

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EXAMINER	
TRAN, JANY	

ART UNIT	PAPER NUMBER
2819	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/655,964	COGDILL ET AL.	
	Examiner	Art Unit	
	JANY TRAN	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/24/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-2, 7-10 and 12-16 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-2, 8, 10, 11-13, 16-20 of U.S. Patent No. 7,307,862. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the application are anticipated by the claims of the patent.

Claim 1 of the present application and claim 1 of Patent No. 7,307,862 are both directed towards a circuit for a memory module address bus comprising a transmission line with a dampening impedance, a branch point, termination impedance and branches.

Claim 2 of the present application and claim 2 of Patent No. 7,307,862 are both directed towards a transmission line that is uni-directional.

Claim 7 of the present application and claim 8 of Patent No. 7,307,862 are both directed towards the termination impedance connected to the dampening impedance.

Claim 8 of the present application and claim 10 of Patent No. 7,307,862 are both directed towards a plurality of memory modules, an address line coupling the memory modules, a transmission line having a series impedance and a parallel impedance in a stub configuration, and the transmission line having a first end coupled to a driver and a second end connected at a point on the address line.

Claim 9 of the present application and claim 12 of Patent No. 7,307,862 are both directed towards the second end of the transmission line is connected at substantially the midpoint of said address line.

Claim 10 of the present application and claim 11 of Patent No. 7,307,862 are both directed towards the transmission line that is uni-directional.

Claim 12 of the present application and claim 16 of Patent No. 7,307,862 are both directed towards where the memory modules is an odd number and the second end of the transmission line is connected to the address line at the middle memory module.

Claim 13 of the present application and claim 17 of Patent No. 7,307,862 are both directed towards where the memory modules is an even number and the second end of the transmission line is connected to the address line at a point substantially midway between two memory modules closest to the mid-point of the address line.

Claim 14 of the present application and claim 18 of Patent No. 7,307,862 are both directed towards a bus controller, a transmission line comprising a series impedance between a driver and a branch point of the transmission line, and a parallel impedance having a first end coupled to the transmission line between the dampening impedance and the branch point and a second end coupled to a termination voltage terminal and the transmission line having branches from the branch point.

Claim 15 of the present application and claim 20 of Patent No. 7,307,862 are both directed towards two branches from the branch point having substantially the same length.

Claim 16 of the present application and claim 19 of Patent No. 7,307,862 are both directed towards the transmission line that is uni-directional.

Claim Objections

Claim 14 is objected to because of the following informalities: There is insufficient antecedent basis for the limitation "dampening impedance" on line 6 of claim 14. For purposes of examination, the Examiner is interpreting the dampening impedance to be the series impedance. Appropriate correction is required.

Claim 22 is objected to because of the following informalities: There is insufficient antecedent basis for the limitation “series resistance” on line 2 of claim 22. For purposes of examination, the Examiner is interpreting the series resistance to be the series impedance. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7-19 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson et al. (US 6,715,014).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Figure 3 of Johnson discloses a circuit for a memory module address bus comprising:

With respect to **claim 1**,

a transmission line (314) comprising a dampening impedance (324) between a driver (312) and a branch point (node between 318 and 320, hereinafter "star node") of said transmission line (314); and

a termination impedance (326) having one end coupled to said transmission line (314) between said dampening impedance (324) and said branch point (star node);

said transmission line (314) having branches (316-322) from said branch point, wherein ones of said branches are coupled to at least one memory module interface (304).

With respect to **claim 2**,

Johnson teaches wherein said transmission line is uni-directional (where the direction is from 312 to star node).

With respect to **claim 3**,

Johnson teaches wherein said ones of said branches are coupled to two memory module interfaces (304, 306).

With respect to **claim 4**,

Johnson teaches wherein said ones of said branches are coupled to three memory module interfaces (302, 304 and 306).

With respect to **claim 5**,

Johnson teaches wherein said ones of said branches are coupled to four memory module interfaces (302, 304, 306 and 308).

With respect to **claim 7**,

Johnson teaches wherein said one end of said termination impedance (end coupled to star node) is connected to said dampening impedance (see Figure 3).

With respect to **claim 8**,

Figure 3 of Johnson further teaches a plurality of memory modules (302-308);

an address line (316-322) coupling said memory modules (302-308);

a transmission line (314) having a series impedance (324) and a parallel impedance (326) in a stub configuration; and

said transmission line (314) having a first end coupled to a driver (312) and a second end connected at a point (star node) on said address line to reduce skew when addressing a memory module.

With respect to **claim 9**,

Johnson teaches wherein said second end of said transmission line is connected at substantially the midpoint of said address line (see Figure 3).

With respect to **claim 10**,

Johnson teaches wherein said transmission line is uni-directional (where the direction is from 312 to star node).

With respect to **claim 11**,

Johnson teaches wherein said parallel impedance (326) is connected to said series impedance (324, see Figure 3).

With respect to **claim 12**,

Johnson teaches wherein said plurality of memory modules is an odd number and wherein said second end of said transmission line is connected to said address line at the middle memory module (Column 2, lines 24-39 and Figure 3).

With respect to **claim 13**,

Johnson teaches wherein said plurality of memory modules is an even number and wherein said second end of said transmission line is connected to said address line

at a point substantially midway between two memory modules closest to the mid-point of said address line (Column 2, lines 24-39 and Figure 3).

With respect to **claim 14**,

Figure 3 of Johnson further teaches a bus controller (inside 312);

a transmission line (314) comprising a series impedance (324) between a driver (312) and a branch point (star node) of said transmission line; and

a parallel impedance (326) having a first end coupled to said transmission line (314) between said series impedance (324) and said branch point (star node) and a second end coupled to a termination voltage terminal (V_{TT});

said transmission line (314) having branches (316-322) from said branch point (star node), wherein ones of said branches are coupled to at least one memory module interface (304).

With respect to **claim 15**,

Johnson teaches wherein two branches (318, 320) of said branches from said branch point have substantially the same length (see Figure 3).

With respect to **claim 16**,

Johnson teaches wherein said transmission line is uni-directional (where the direction is from 312 to star node).

With respect to **claim 17**,

Johnson teaches wherein said ones of said branches (316) are coupled to two memory module interfaces (304 and 306).

With respect to **claim 18**,

Johnson teaches wherein said ones of said branches are coupled to three memory module interfaces (302, 304 and 306).

With respect to **claim 19**,

Johnson teaches wherein said ones of said branches are coupled to four memory module interfaces (302, 304, 306 and 308).

With respect to **claim 21**,

Johnson teaches wherein said first end of said parallel impedance (326) is connected to said series impedance (324, at star node).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 6 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson in view of Buuck et al. (US 5,583,449).

With respect to **claim 6**,

Figure 3 of Johnson discloses the circuit as claimed, but is silent to wherein the distance from said branch point to said one end of said termination impedance is greater than the length of said branches.

Figure 2 of Buuck teaches a circuit for cancelling reflections on a transmission line that includes having the distance (L_1) between a branch point (80) and one of the devices (20 or 30) to be less than the overall distance between the driver and the device (sum of L_1 and L_2) for reducing electromagnetic interference (Abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the distances from a branch point to the end of the termination impedance to be greater than the length of the branches as taught by Buuck to reduce electromagnetic interference (Abstract).

With respect to **claim 20**,

Figure 3 of Johnson discloses the circuit as claimed, but is silent to wherein the distance from said branch point to said first end of said parallel impedance is greater than the length of said branches.

Figure 2 of Buuck teaches a circuit for cancelling reflections on a transmission line that includes having the distance (L_1) between a branch point (80) and one of the devices (20 or 30) to be less than the overall distance between the driver and the device (sum of L_1 and L_2) for reducing electromagnetic interference (Abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the distances from a branch point to the end of the

termination impedance to be greater than the length of the branches as taught by Buuck to reduce electromagnetic interference (Abstract).

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson in view of Mizukami et al (US 5,111,080).

With respect to **claim 22**,

Figure 3 of Johnson discloses the circuit as claimed, but is silent to wherein said parallel impedance and said series impedance are mounted on opposite sides of a printed circuit board.

Figure 3 of Mizukami teaches a signal transmission circuit with impedance matching circuitry that includes a parallel impedance (R4) and a series impedance (R1) that are mounted on opposite sides (left and right sides) of a printed circuit board (Figure 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to mount resistors on opposite sides of the printed circuit board as taught by Mizukami because placement of resistors is a choice of design and there is no difference in terms of impedance matching or reduction of signal levels.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JANY TRAN whose telephone number is (571) 270-5074. The examiner can normally be reached on Monday - Friday, 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jany Tran/
Examiner, Art Unit 2819

/Rexford N BARNIE/

Supervisory Patent Examiner, Art Unit 2819